UNITRODE

UC17131/2/3
UC27131/2/3
UC37131/2/3

Smart Power Switch

PRELIMINARY

FEATURES

- 300mA Continuous Output Current
- Low Side or High Side Switch Configuration
- 8V to 65V Operation
- Overload and Short Circuit Protection
- Power Interruption Protection
- +6V Regulated Voltage
- 1V Saturation Voltages
- 2mA Quiescent Current
- Programmable Overcurrent and Power Interruption Protection (on UC37132)
- 1% to 30% Programmable Input Comparator Hysteresis (on UC37132)
- Low and High Side Internal Clamps When Driving Inductive Loads

DESCRIPTION

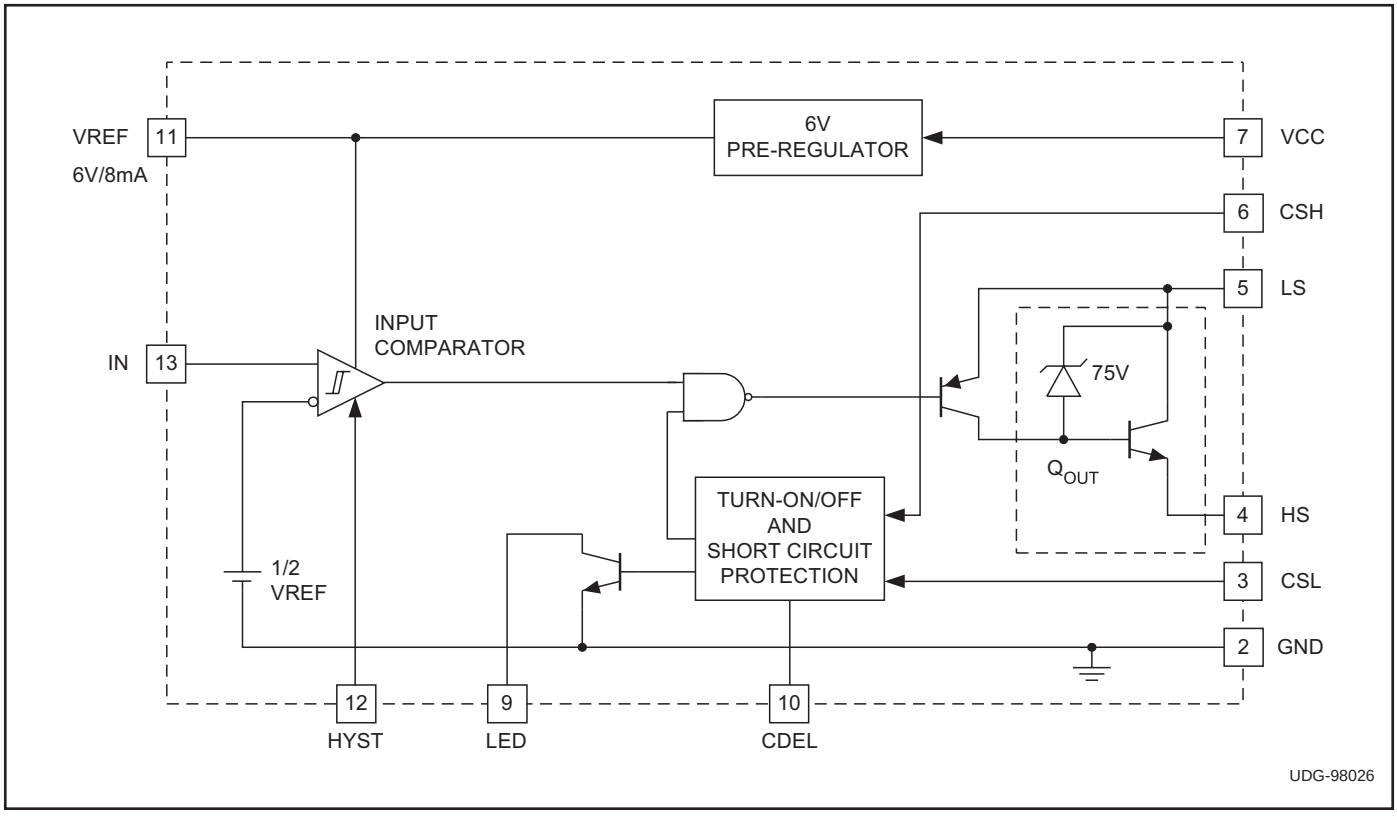
The UC37131, UC37132 and UC37133 are a family of smart power switches which can drive resistive or inductive loads from the high side or low side.

The UC37132 is a 14 pin package device which can accomodate both low side (load to V_{CC}) or high side (load to GND) configurations. The UC37131 and UC37133 are exclusively for a low side or a high side configuration respectively and both are available in an 8 pin package. Both high side and low side configurations provide high current switching with low saturation voltages which can drive resistive or inductive loads.

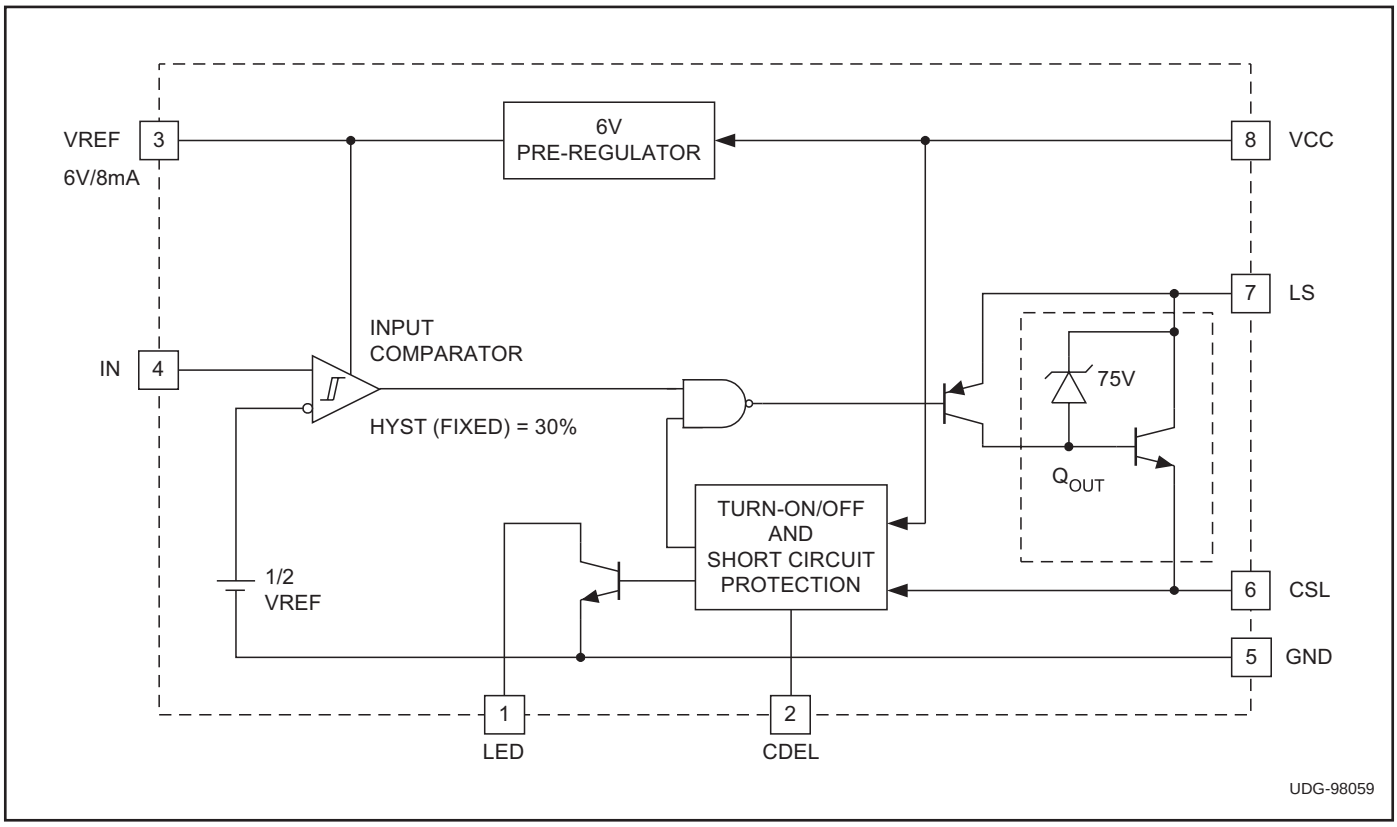
The input to the switch is driven by a low voltage signal, typically 5V. Additionally, UC37132 features adjustable hysteresis. The output of the device can switch a load between 8V and 65V. Output current capability is 300mA continuous or 600mA peak.

The device also has inherent smart features that allow for programmable turn on delay in enabling the output following startup. The same capacitor that specifies the turn on delay is also used to program a V_{CC} power interruption time. If V_{CC} drops below a threshold for a time specified by this capacitor, the output is turned off and a new turn on delay will be re-triggered. Similarly, if high current persists longer than the response delay, the output driver will operate in a very low duty cycle mode to protect the IC.

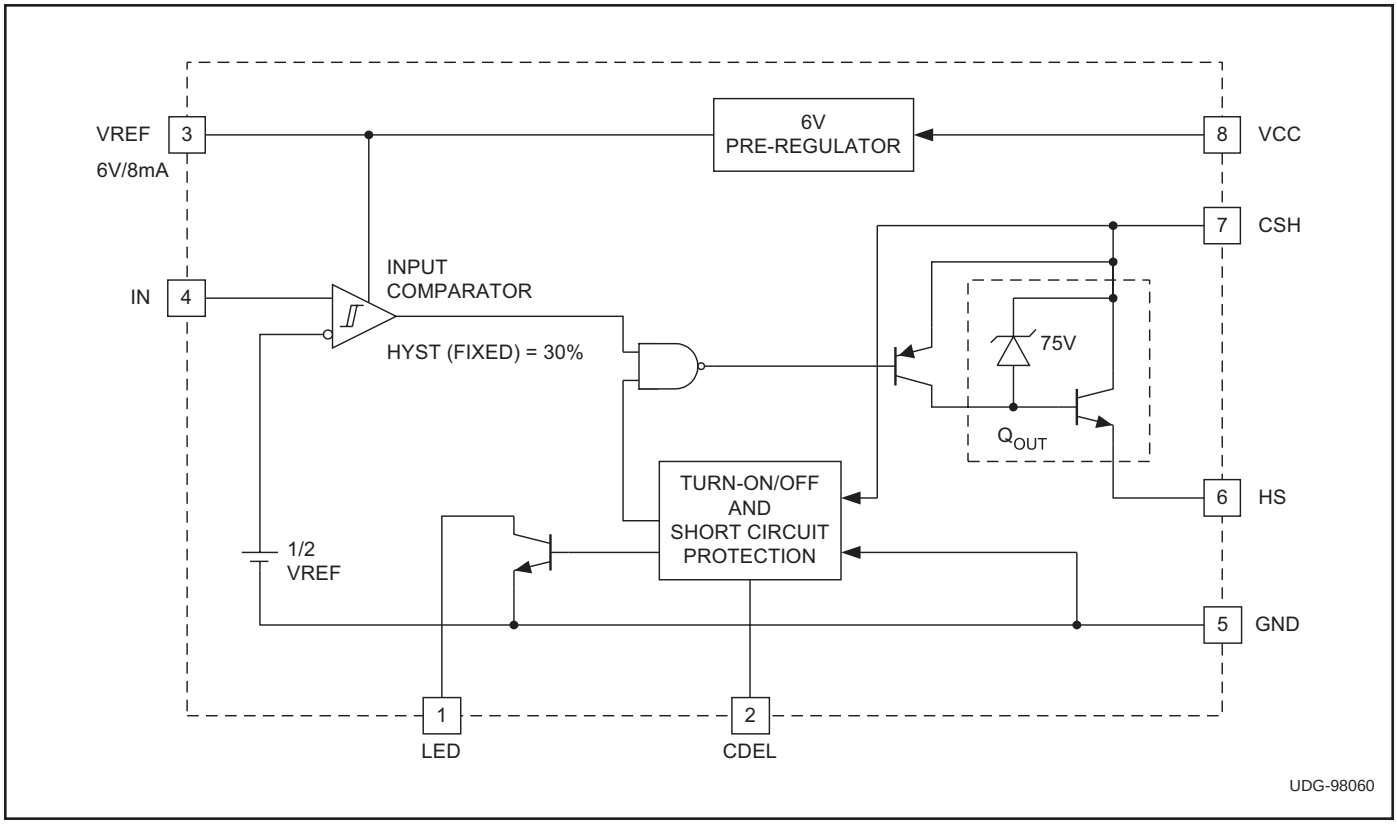
UC37132 BLOCK DIAGRAM



UC37131 BLOCK DIAGRAM



UC37133 BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{CC} 65V
LS – HS 90V
LS 90V
CSH, LED 65V
Output Current
  Continuous 300mA
  Peak 600mA
Remaining Pin Voltages . . . . . –0.3V to 9V
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

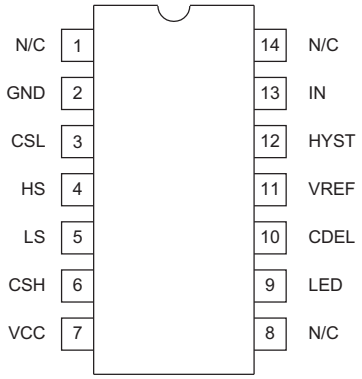
PRODUCT SELECTION TABLES

PART NUMBER	CONFIGURATIONS	PACKAGE PIN COUNT
UCX7131	Low Side Only	8
UCX7132	Low Side or High Side	14
UCX7133	High Side Only	8

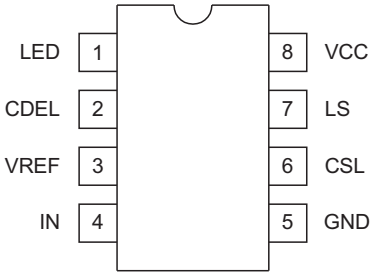
PART NUMBER	TEMPERATURE RANGE	AVAILABLE PACKAGES
UC1713X	–55°C to +125°C	J
UC2713X	–40°C to +85°C	D, N
UC3713X	0°C to +70°C	D, N

CONNECTION DIAGRAMS

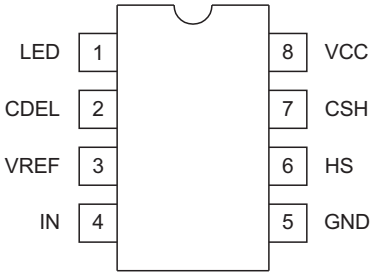
DIL-14, SOIC-14 (Top View)
(for UCX7132)
J, N, or D Packages



DIL-8, SOIC-8 (Top View)
(for UCX7131)
J, N, or D Packages



DIL-8, SOIC-8 (Top View)
(for UCX7133)
J, N, or D Packages



ELECTRICAL CHARACTERISTICS

Unless otherwise specified, CDEL = 10nF, V_{CC} = 25V, CSL = GND, CSH = LS; R_{CSH} = 0.5Ω (Note 1); IN=0V (for OFF condition) and IN=5V (for ON condition); $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Reference					
VREF	25°C	5.8	6	6.2	V
	–55°C to 125°C	5.6	6	6.4	V
Line Regulation	V_{CC} = 8V to 64V		10	50	mV
Load Regulation	0 < I_{REF} < 8mA		10	50	mV
Short Circuit Current	REF = 0V		20	35	mA
Input Comparator					
Turn on Threshold Voltage			3		V
Input Bias Current	V_{IN} = 3.5V			5	µA
Hysteresis	R_{HYST} = GND (Internally for X31, X33)		0.9		V
	R_{HYST} = 96.67k for (X32)		30		mV

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PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output: High Side (UCX7133: CSH = LS and CSL = GND Internally)					
Rise Time (Off to On)	R_{LOAD} = 250Ω to GND		20		V/µs
Fall Time (On to Off)	R_{LOAD} = 250Ω to GND		5		V/µs
Output Short Circuit	HS = GND		600		mA
Saturation Voltage	25°C R_{LOAD} = 100Ω to GND			1	V
	–40°C, R_{LOAD} = 100Ω to GND			1.2	V
	–55°C, R_{LOAD} = 100Ω to GND			1.3	V
Leakage Current				5	µA
Output: Low Side (UCX7131; CSH = Vcc and CSL = HS Internally; See Figure 2b)					
Rise Time (On to Off)	R_{LOAD} = 250Ω to V_{CC}, R_{CSL} = 0.5Ω		5		V/µs
Fall Time (Off to On)	R_{LOAD} = 250Ω to V_{CC}, R_{CSL} = 0.5Ω		20		V/µs
Output Short Circuit	LS = V_{CC}		600		mA
Saturation Voltage	25°C, R_{LOAD} = 100Ω to V_{CC}, R_{CSL} = 0.5Ω			1	V
	–40°C, R_{LOAD} = 100Ω to V_{CC}, R_{CSL} = 0.5Ω			1.2	V
	–55°C, R_{LOAD} = 100Ω to V_{CC}, R_{CSL} = 0.5Ω			1.3	V
Leakage Current				5	µA
V_{CC} Fault Section					
Output Turn On Delay, $t_{D(ON)}$	Step V_{CC} from 0V to 8V (See Figure 3a)		12.8		ms
Output Turn Off Delay, $t_{D(OFF)}$	Pulse V_{CC} = 25V to 0V (See Figure 3b)		500		µs
V_{CC} Turn Off Threshold	Pulse V_{CC} Low		7		V
Overcurrent Fault Section (See Figure 3c)					
Short Circuit Turn-Off Delay, t_{SC}	Step $I_{LOAD:}$ 0mA to 400mA		75		µs
Short Circuit Recovery Time, t_{ROFF}	I_{LOAD} = 400mA, 100µS		10		ms
High Side Current Threshold, I_{TH-H}	R_{CSH} = 0.5Ω		300		mA
Low Side Current Threshold, I_{TH-L}	R_{CSL} = 0.5Ω		300		mA
LED Output					
I_{SINK}, t_{DOFF}, t_{ROFF}			3		mA
$I_{LEAKAGE}$			1		µA
Overall					
Delay to Output			2		µs
ICC	Output Off			2	mA
	I_L = 1mA, 250mA (High and Low Side)			3	mA

Note 1: All test conditions are for a high side configuration as in Figure 2a, unless otherwise specified.

PIN DESCRIPTIONS

CDEL: A capacitor connected to this pin is used to program both V_{CC} pulse interruption time and power turn-on delay. The capacitor discharge time corresponds to V_{CC} interruption and the charge time to V_{CC} turn-on delay. The ratio between turn-on delay and turn-off delay will be fixed based on internal charge and discharge currents and voltage thresholds.

The same fault circuitry and capacitor is used for short circuit and overload protection. If an overcurrent or short circuit is detected, the capacitor starts charging and turns off the output if the condition persists at the end of its charge time. The output then will operate in a low-duty cycle mode to protect the IC. After short circuit recovery, the output will be reactivated in order to check if the short circuit was removed or not. If the overcurrent persists the chip will continue in this pulsing mode.

PIN DESCRIPTIONS (continued)

CSH: (For UC37132 and UC37133) This high side current sense pin is used to program the current limit for high side applications by connecting a resistor between V_{CC} and CSH. An over load current is detected when the voltage drop between V_{CC} and CSH exceeds 150mV.

CSL: (For UC37131 and UC37132) This low side current sense pin is used to program the current limit for low side applications by connecting a resistor between CSL and GND. An over load current is detected when the voltage drop between CSL and GND exceeds 150mV.

GND: The reference point for the internal reference, all thresholds, and the return for the remainder of the device.

HS: (For UC37132 and UC37133) The output of the switching transistor in the high side configuration. The emitter of the output transistor is the HS pin which is connected to the load.

HYST: (For UC37132) The pin used to program the input comparator hysteresis by connecting a resistor to ground. The hysteresis defaults to 30% with HYST grounded (internally for UC37131 and UC37133).

$$V_{HYST} = \frac{3000}{(3330 + R_{HYST})}$$

IN: The input to the comparator that detects when the output transistor should be turned on. The input threshold is 3.0V (1/2 VREF) and the input voltage range is 0V to V_{REF}.

LED: Open collector output intended to drive an LED during overcurrent and power interrupt faults (see Figures 3b and 3c).

LS: (For UC37131 and UC37132) The output of the switching transistor in the low side configuration. The collector of the output transistor is the LS pin which is connected to the load.

VREF: The 6V regulated reference capable of supplying up to 8mA. The recommended decoupling capacitor is 0.1µF.

VCC: The supply voltage for the chip. Decouple this pin with a good quality ceramic capacitor to ground.

DESCRIPTION OF OPERATION

Reference

The UC37131/2/3 family of devices features a 6V bandgap reference that is used to bias on chip logic. Although the 6V reference is not trimmed, this bandgap reference provides less than 200ppm/°C. It is also used to generate the on chip 3V input comparator threshold and is needed for the programmable hysteresis. The on chip reference has 8mA maximum current sourcing capacity that is designed to power up external circuitry.

Input Comparator

The input comparator is a high gain comparator with hysteresis that fully switches with either a small signal (40mV, minimum for 1% hysteresis) or a logic signal (0 to 6V max). A 5mV overdrive of the 3V threshold is only needed to switch the driver.

The hysteresis is set to 30% on the UC37131 and UC37133. (This is 30% of 3V equating to 0.9V of hysteresis.) On the UC37132 it is programmable from 1% to 30%.

Fault Logic

The output of the comparator is logic ANDed with the output of the fault logic. If a fault, either a power interrupt or an overcurrent condition, persists longer than it takes for the CDEL to discharge from its V_{CLAMP} level of 5.7V to its V_{FAULT_L} of 1.1V, the fault protection block will output a logic 0 to the AND gate and turn off the output driver. If the fault goes away prior to CDEL being discharged to 1.1V, the chip will resume normal operation.

The power interrupt normal operation consists of the chip turning the driver immediately back on if the interrupt goes away prior to CDEL reaching its lower threshold as described above. If the power stays off longer than this time, then a power up delay will be initialized once power is resumed. This delay is the time it takes for CDEL to charge from 0V to V_{FAULT_H} of 5.1V.

The overcurrent fault normal operation consists of the chip staying off until CDEL fully recharges to V_{FAULT_H} of 5.1V. This is $t_{R(OFF)}$. Once CDEL reaches 5.1V, the driver will turn back on. If the overcurrent fault is still present, the chip will operate in a very low duty cycle based on the discharge (driver on) and charge time (driver off) of the CDEL capacitor. This overcurrent timing makes the chip act "smart" by allowing very high currents needed to drive large capacitive loads without setting off an overcurrent fault.

An active low open collector output, LED, indicates a fault by going low "after" the CDEL has been discharged all the way to V_{FAULT_L} of 1.1V.

DESCRIPTION OF OPERATION (continued)

Output Driver

Once the turn-on signal is gated through from the input comparator, the output transistor is turned on. The output drive transistor is a composite PNP, NPN structure. This is a specially designed structure that keeps all the drive current needed for the load to be sourced through the LS pin. This keeps the overall power dissipation to less than 3mA independent of the load.

The overcurrent and current limit thresholds are programmed with the resistor R_{CSH} from CSH to VCC (high side) or R_{CSL} from CSL to GND (low side). For example, a 150mV ($I_{LOAD} \bullet R_{CSH}$) threshold will set the high side overcurrent fault threshold. An overall short circuit protection threshold is set at 300mV. Therefore, the recommended R_{CSH} of 0.5Ω will result in the 600mA short circuit. By changing the R_{CSH} value the user can optimally set the overcurrent and short circuit current limits for his application.

The output driver also has a 75V zener diode wired between its base and collector. This allows the output to swing and clamp to 75V above ground when discharging an inductive load in a low side application. This consequently allows the LS pin to safely swing above VCC. Similarly, the 75V zener diode will allow the HS pin to safely swing and clamp 75V below LS/VCC when discharging an inductive load in a high side application. This 75V zener diode simplifies the user application by eliminating the need for external clamp diodes.

APPLICATION INFORMATION

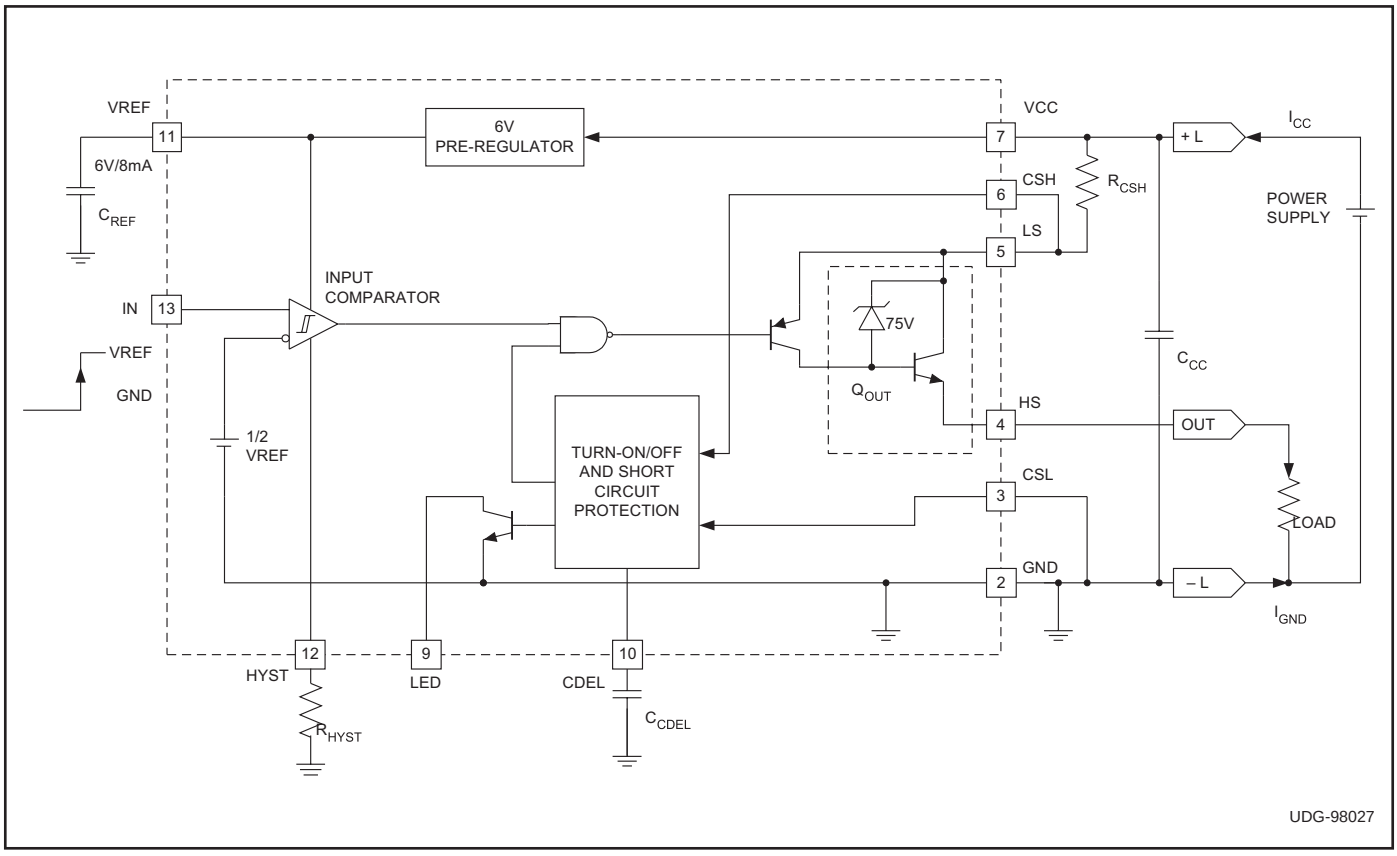

Figure 2a. High Side Application

APPLICATION INFORMATION (continued)

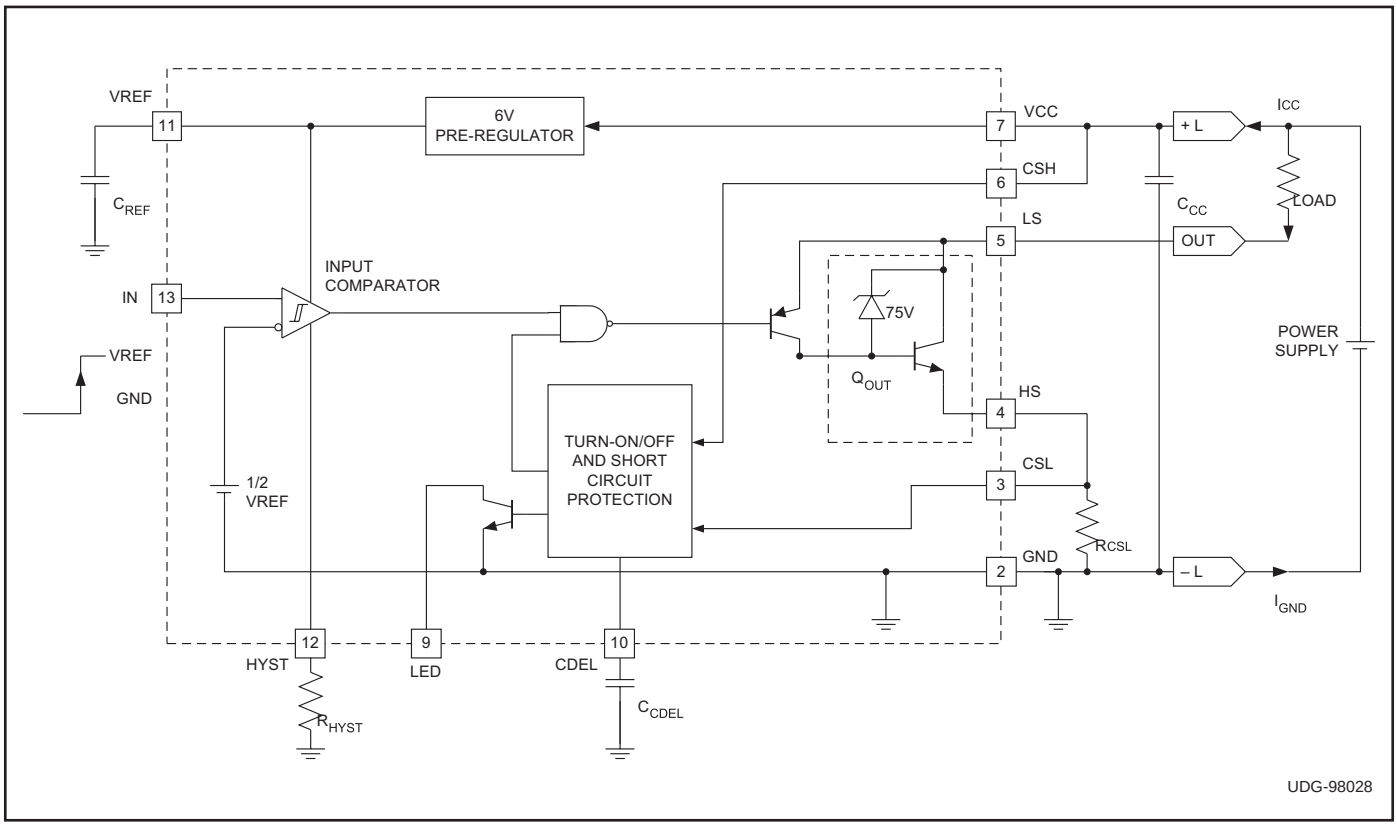

Figure 2b. Low Side Application

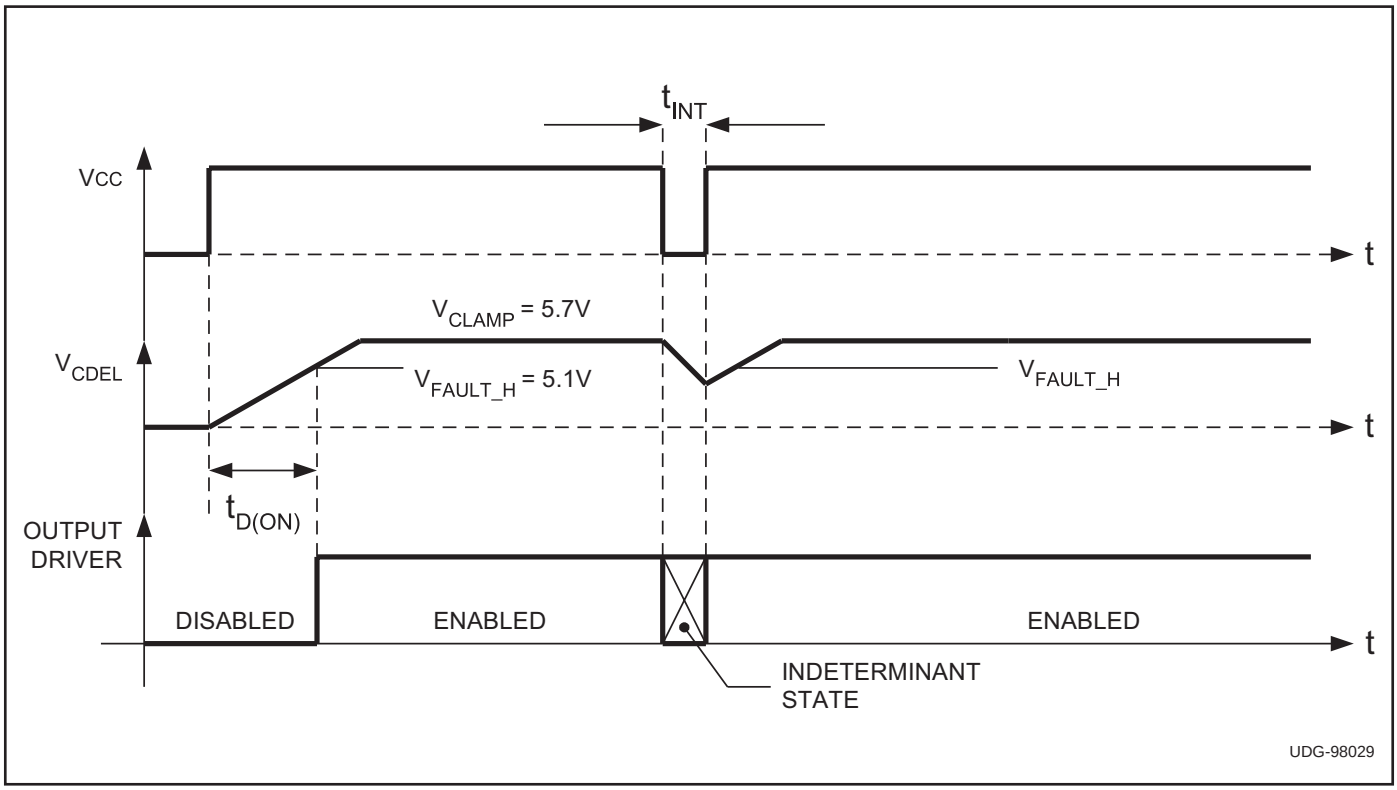

Figure 3a. Power Interrupt Ignore Operation

APPLICATION INFORMATION (continued)

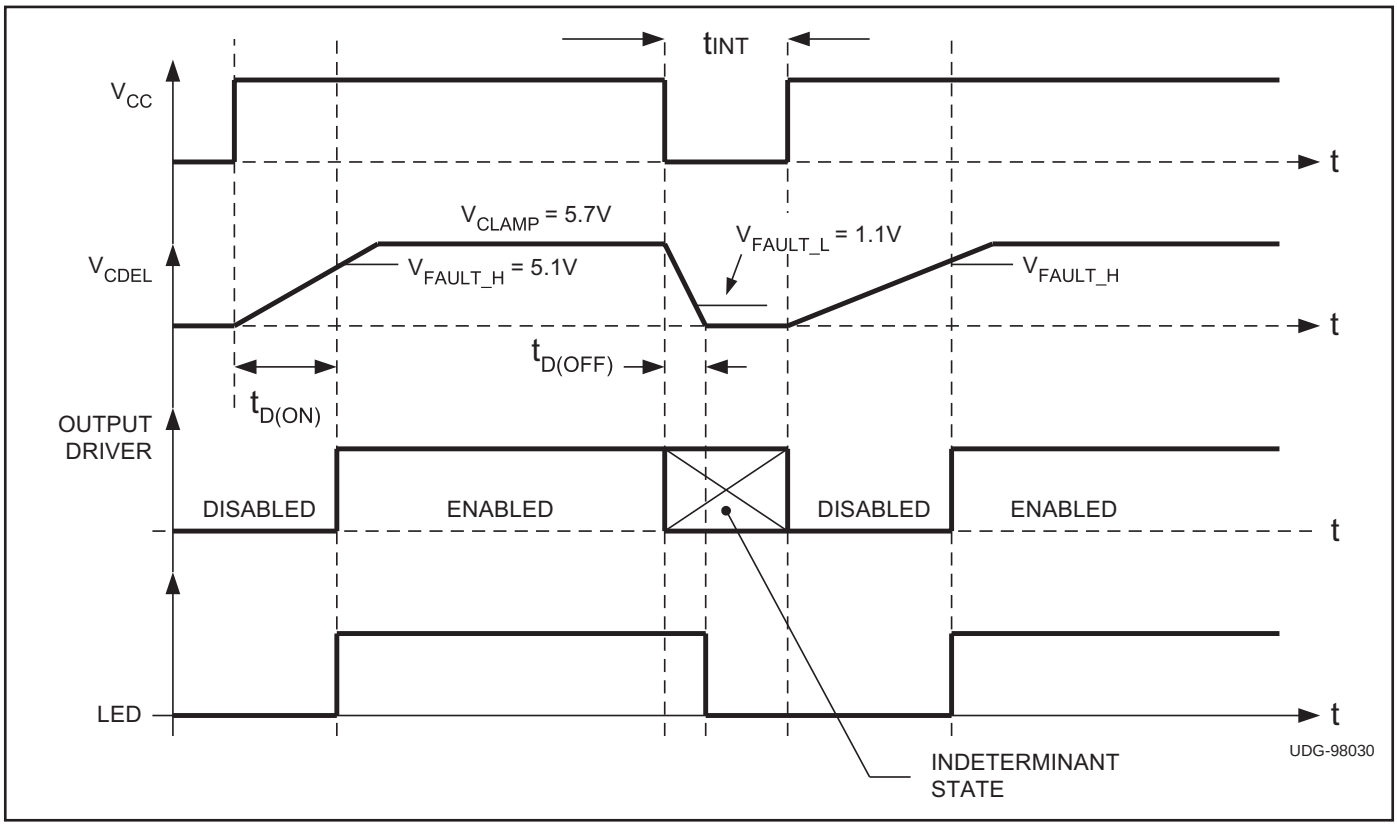

Figure 3b. Power Interrupt Fault Operation

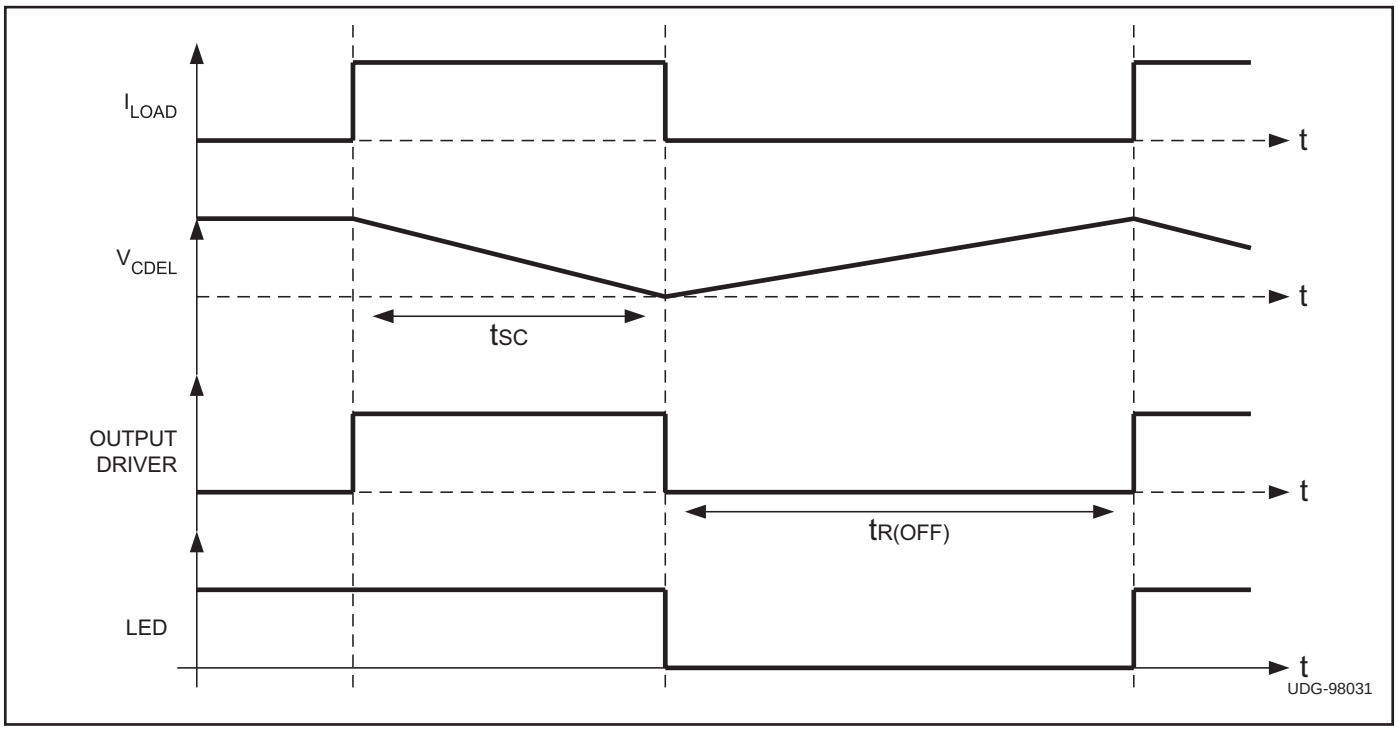

Figure 3c. Overcurrent Fault Operation

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